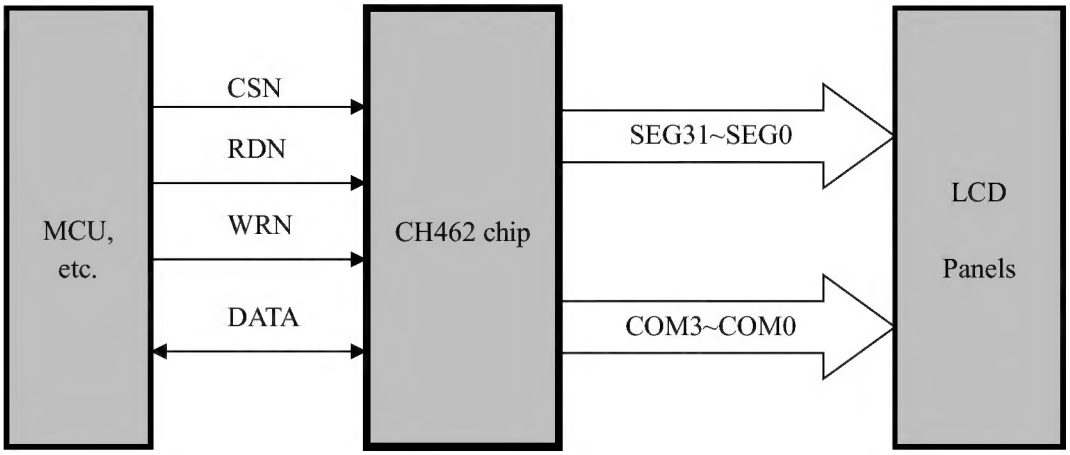
LCD display driver chip CH462

Datasheet
Version: 1B
http://wch.cn

1. Overview

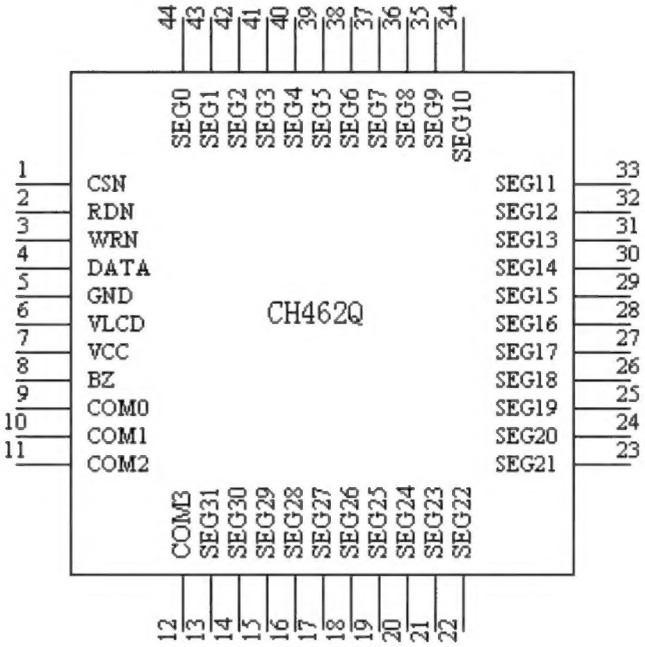
CH462 is LCD display driver chip. CH462 has built-in clock oscillator circuit, and supports 128 (32×4) LCD panel.

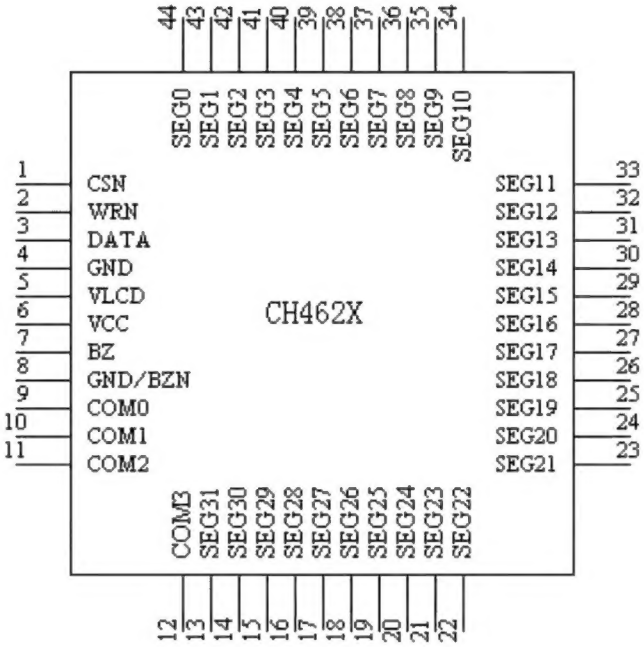


2. Features

- Max. support 32×4 LCD panel, 32 SEG and 4 COM
- 1/2 or 1/3 bias, 1/2 or 1/3 or 1/4 duty LCD display application can be selected
- Provide VLCD pin, used to adjust the LCD working voltage
- Built-in bias circuit
- Built-in clock oscillator circuit
- 2 optional buzzer frequencies (2KHz or 4KHz)

3. Package





Package	Width		Pitch of Pin		Instruction of Package	Ordering information
LQFP44	10*10mm		0.8mm	31.5mil	Standard LQFP 44-pin patch	CH462Q
LQFP44	10*10mm		0.8mm	31.5mil	Standard LQFP 44-pin patch	CH462X

4. Pins

CH462Q Pin No.	CH462X Pin No.	Pin name	Type	Pin description
1	1	CSN	Input	Chip selection signal, active low, built-in pull-up resistor
2	None	RDN	Input	Read clock, built-in pull-up resistor, data latch output during falling edge
3	2	WRN	Input	Write clock, built-in pull-up resistor, latch data during rising edge
4	3	DATA	Input/output	Data signal, tri-status and bi-directional
5	4, 8	GND	Power	Common ground
6	5	VLCD	Power	LCD power supply input
7	6	VCC	Power	Working power supply input
8	7	BZ	Output	Buzzer output
9~12	9~12	COM0~COM3	Output	LCD COM driver port
44~13	44~13	SEG0~SEG31	Output	LCD SEG driver port

5. Functional Specification

5.1. General Specification

For data in this manual, those ending with B are binary numbers and those ending with H are hexadecimal numbers. Otherwise, they are decimal numbers. The bit marked as x indicates that the bit can be any value.

5.2. LCD Display Driver

CH462 is built with 32×4 bits data storage and 32 half-byte units with the addresses from 00H to 1FH, which correspond to the LCD light connected by SEG and COM pins respectively. The corresponding relations are as follows:

Addressing	COM3	COM2	COM1	COM0
SEG0(00H)	D3	D2	D1	D0
SEG1(01H)	D3	D2	D1	D0
|	|	|	|	|
SEG15(0FH)	D3	D2	D1	D0
SEG16(10H)	D3	D2	D1	D0
|	|	|	|	|

SEG30(1EH)	D3	D2	D1	D0
SEG31(1FH)	D3	D2	D1	D0

Related configuration commands are as follows

Name	Command code	Operation number	Functional Description
SYS OFF	100	0000-0000-X	Turn off system oscillator, turn off LCD
LCD OFF	100	0000-0010-X	Turn off LCD display
LCD ON	100	0000-0011-X	Turn on LCD display
BIAS, DUTY	100	0010-abXc-X	ab=00: 2 COMS(COM0~COM1) ab=01: 3 COMS(COM0~COM2) ab=10: 4 COMS(COM0~COM3) c=0: 1/2 BIAS c=1: 1/3 BIAS

5.3. BZ Buzzer Control

Support 2 optional buzzer (2KHz or 4KHz) outputs. BZ pins output low level by default.

Name	Command code	Operation number	Functional Description
BZ OFF	100	0000-1000-X	Turn off BZ output
BZ ON	100	0000-1001-X	Turn on BZ output
BZ 4KHZ	100	010X-XXXX-X	BZ frequency selection: 4KHZ
BZ 2KHZ	100	011X-XXXX-X	BZ frequency selection: 2KHZ

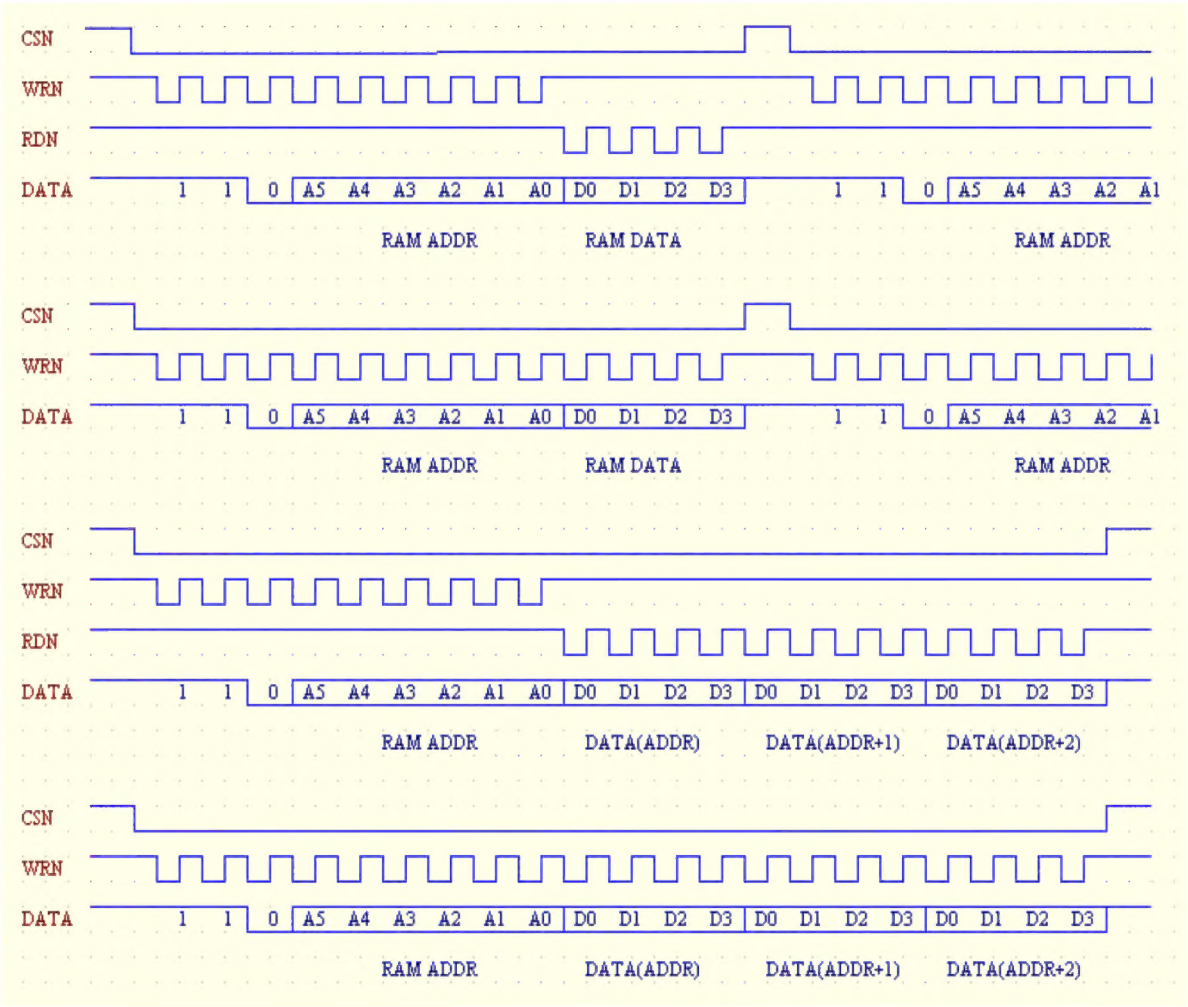
5.4. Serial Interface

CH462 supports 4 kinds of command modes. The command code needs to be added before data or command code transmission. The command code only needs to be added for the first one, the address will be automatically added by one during data transmission, and CSN needs to be pulled up upon the completion of a single transmission, so that the previous command mode will be reset, once the CSN is pulled down, the new mode work will be transmitted at first.

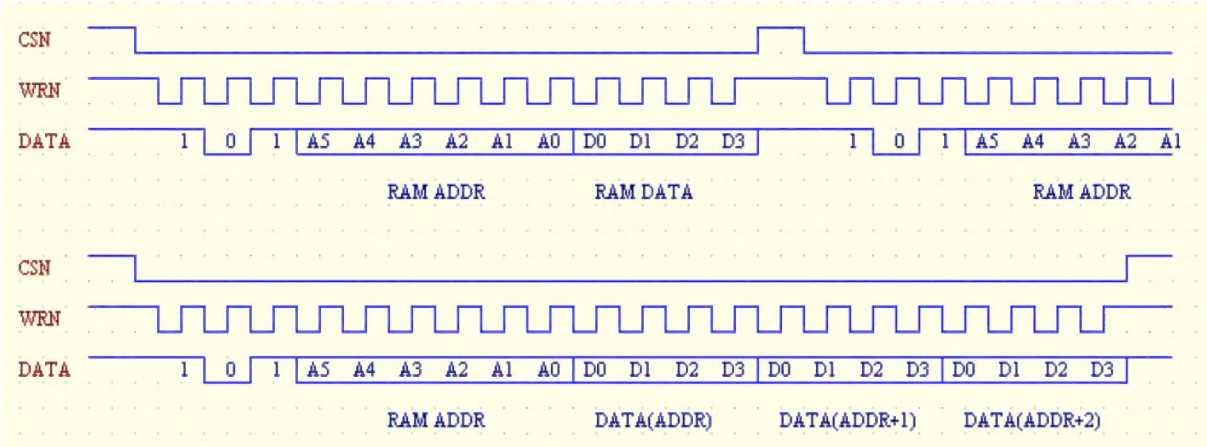
Operation mode	Command code
Read	110
Write	101
Read modify write	101(111)
Order	100

CSN serves as a chip selection signal, which can reset the serial port circuit when it is in high level and communicate with MCU when it is in low level. RDN is a read clock signal, and the data is latched on its falling edge and output to the DATA line. WRN is a write clock signal, and the data on the DATA line is latched on its rising edge. The RDN line can also be omitted, where WRN replaces the read clock (read modify write command code is changed to 111).

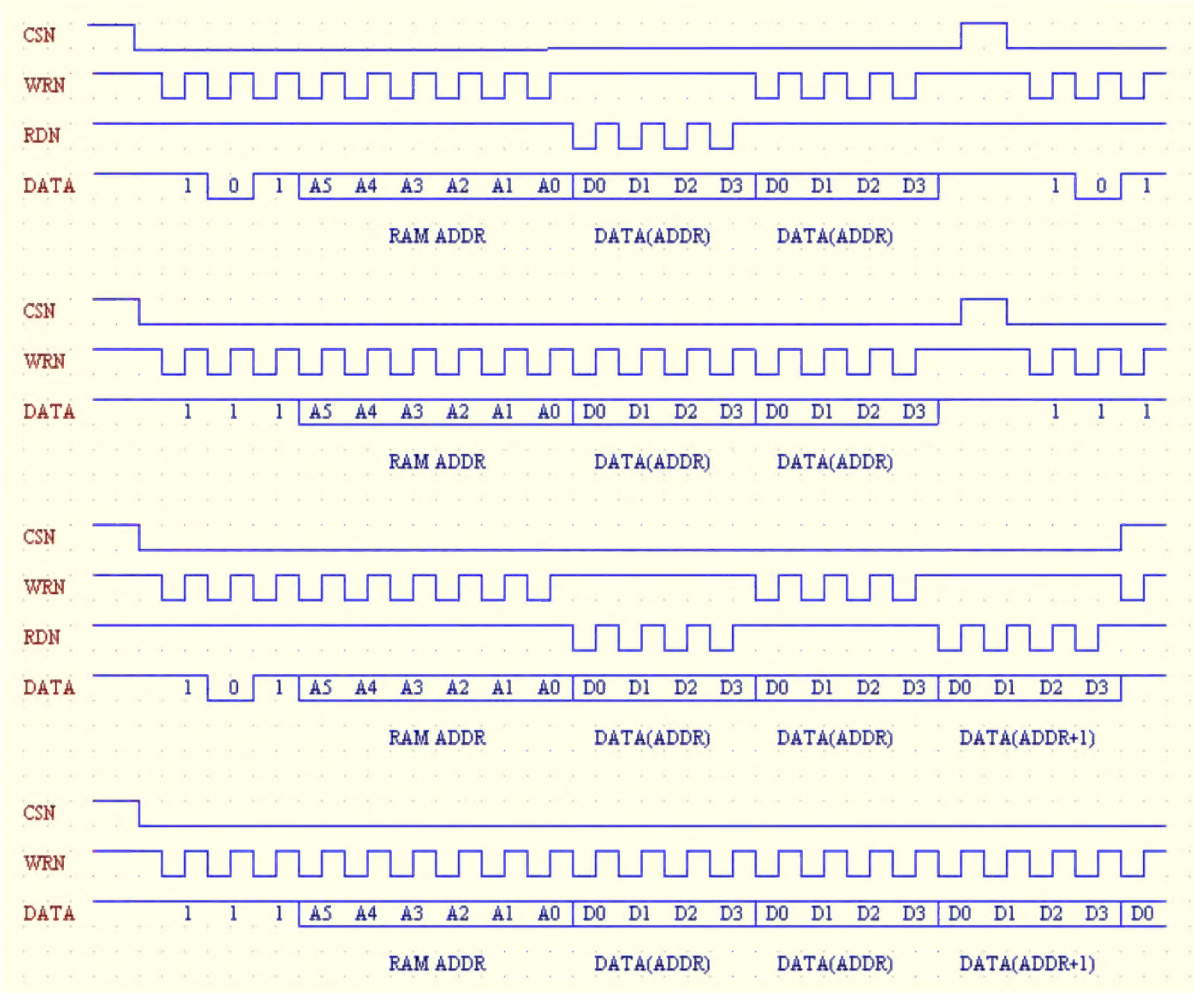
Read operation:



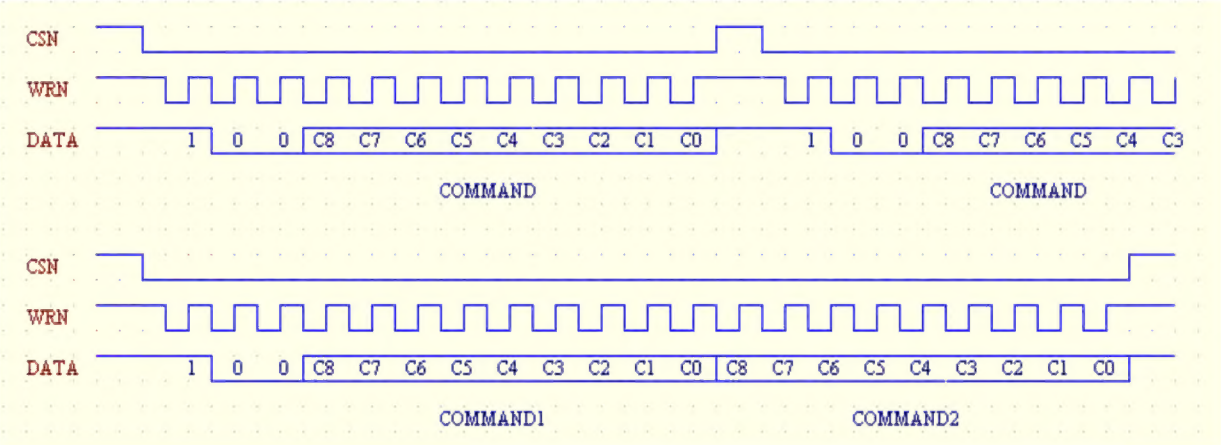
Write operation:



Read modify write:



Configuration command:



6. Command Table

Name	Command code	Operation number	Functional Description
Read	110	A5A4A3A2A1A0D0D1D2D3	Read display RAM
Write	101	A5A4A3A2A1A0D0D1D2D3	Write display RAM
Read modify write	101(111)	A5A4A3A2A1A0D0D1D2D3	Read display RAM, modify, write display RAM
SYS OFF	100	0000-0000-X	Turn off system oscillator, turn off LCD
SYS ON	100	0000-0001-X	Turn on system oscillator
LCD OFF	100	0000-0010-X	Turn off LCD display
LCD ON	100	0000-0011-X	Turn on LCD display
BZ OFF	100	0000-1000-X	Turn off BZ output
BZ ON	100	0000-1001-X	Turn on BZ output
BIAS, DUTY	100	0010-abXc-X	ab=00: 2 COMS(COM0~COM1) ab=01: 3 COMS(COM0~COM2) ab=10: 4 COMS(COM0~COM3) c=0: 1/2 BIAS c=1: 1/3 BIAS
BZ 4KHZ	100	010X-XXXX-X	BZ frequency selection: 4KHZ
BZ 2KHZ	100	011X-XXXX-X	BZ frequency selection: 2KHZ

Notes: X: Arbitrary value. A5~A0: RAM address. D3~D0: RAM data

7. Parameters

7.1. Absolute Maximum Value

Name	Parameter description	Min.	Max.	Unit
TA	Ambient temperature during operation	-40	85	℃
TS	Ambient temperature during storage	-55	125	℃
VCC	Supply voltage (VCC is connected to the power supply, GND is grounded)	-0.5	6.0	V
VIO	Voltage on the input or output pins	-0.5	VCC+0.5	V
VLCD	LCD voltage	-0.5	VCC+0.5	V

7.2. Electrical Parameters

Test Conditions: TA=25℃, VCC=5V

Name	Parameter description	Min.	Typ.	Max.	Unit
VCC	Power supply voltage	3	5	5.5	V
VLCD	LCD voltage	0		VCC	V
ICC	Working current (LCD ON, BZ OFF)		300		uA
Islp5	5V quiescent current		6		uA
Islp3	3.3V quiescent current		3		uA

Io1	LCD drive current		200		uA
Io2	BZ drive current		2		mA
VOL	Low level input voltage	0		0.7	V
VOH	High level input voltage	2.0		VCC	V

7.3. Internal Timing Parameters

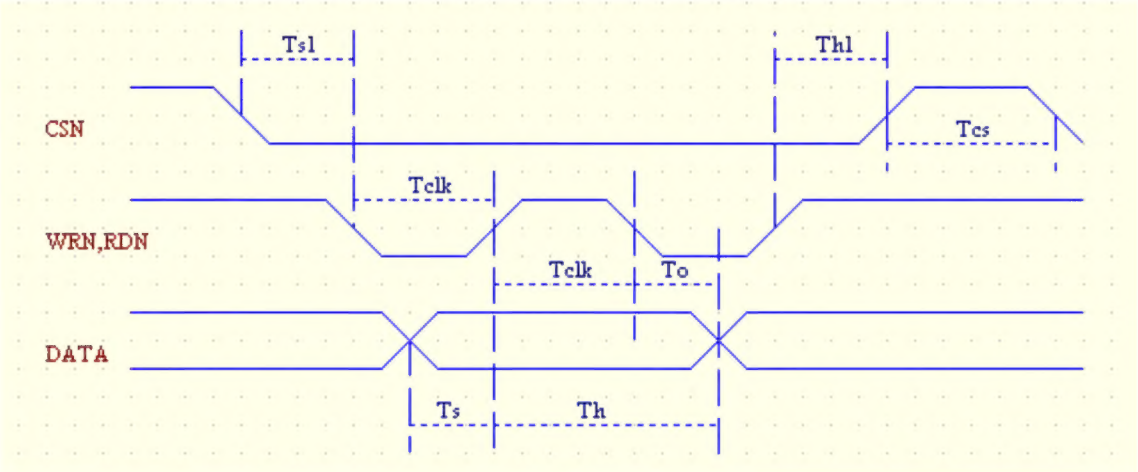
Test Conditions: TA=25℃, VCC=5V

(Note: The timing parameters in this table are multiples of the built-in clock cycle, and the frequency of the built-in clock may be affected by the supply voltage)

Name	Parameter description	Min.	Typ.	Max.	Unit
TPR	Power on reset time	3	10	50	mS
Fosc	Oscillation frequency		256		KHz
Fbz1	BZ(2KHz)	1.5	2	2.5	KHz
Fbz2	BZ(4KHz)	3	4	5	KHz
Flcd	LCD frequency		Fosc/1024		Hz
Tcom	LCD COM cycle		n/Flcd		S

7.4. Interface Timing Parameters

Test Conditions: TA=25℃, VCC=5V, refer to the attached figure



Name	Parameter description	Min.	Typ.	Max.	Unit
Ts1	CSN to WRN, setup time of RDN falling edge	200			nS
Th1	CSN to WRN, holding time of RDN rising edge	200			nS
Tcs	Serial interface reset pulse width	200			nS
Tclk	High and low level width of WRN, RDN clock signal	200			nS
Ts	Setup time of DATA to WRN rising edge	50			nS
Th	Hold time of DATA to WRN rising edge	20			nS
To	Delay of valid DATA output to RDN or WRN falling edge			100	nS